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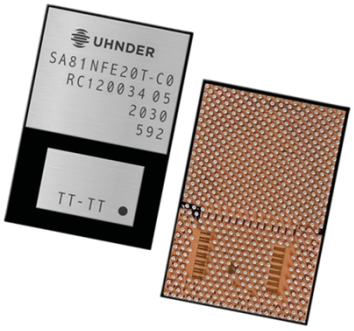
S81

Low Cost 4D Digital Imaging Radar
Product Technical Brief



Overview

The S81 is a low cost, fully software defined 4D Imaging Radar-on-Chip (RoC) with Digital Code Modulation (DCM), certified for use in key automotive safety applications such as automatic emergency braking, lane change assist, adaptive cruise control, and blind-spot detection, as well as automated driving functions for autonomous vehicles.

The RoC uses a PMCW (phase modulated continuous wave), MIMO (multiple-input multiple-output) radar architecture capable of processing up to 96 virtual channels. It supports 12 transmit antenna channels (Tx) and 8 receive antenna channels (Rx). The S81 has built-in processors to run a full radar stack, including application and OEM-specific software on chip.

The DCM-based imaging radar provides a rich point cloud output for use in long, mid, and short-range applications with high contrast resolution (HCR) to deliver maximum discrimination and high-confidence detection of independent small targets. Furthermore, the DCM technology enables improved interference mitigation and is inherently hack resistant to spoofing.

The RoC is provided with system tools and production-ready software APIs to enable quick time-to-market for customers.

Key Features

- 76-81 GHz Frequency Range
- 4D Digital Imaging Radar: Simultaneous Measurement of Range, Velocity, Azimuth, and Elevation Angle
- Up to 96 Virtual Receive Channels (VRx) – True MIMO
  - 8 Receive Antenna Channels (Rx)
  - Up to 12 Transmit Antenna Channels (Tx)
- High Contrast Resolution
- Hack Resistant to Radar Spoofing
- Software Defined Frame and Scan Configuration
- Advanced Interference Mitigation
- AEC-Q104 Qualified
- Supports ASIL-B Functional Safety (ISO 26262)
- Supports user Algorithms On-Chip with High Performance CPU and DSP Cores
- ASPICE Qualified SDK with Ready-to-Integrate APIs
- Small Form Factor
- Low Power Consumption
- Supports Multichip Cascading

Target Applications

- Imaging Radar for Automated Driver Assistance Systems (ADAS). Examples:
  - Pedestrian Automatic Emergency Braking (P-AEB)
  - Lane Change Assist (LCA)
  - Blind Spot Detection (BSD) and Cross-Traffic Detection (CTD)
- Autonomous Vehicles (AVs)

Key Specifications

S81 Radar-on-Chip (RoC)	Value
Center Frequency	76 – 81 GHz
Channels	Up to 12 Tx & 8 Rx
Tx Output Power[1]	12 dBm
Maximum Modulation Bandwidth	1 GHz
Noise Figure (NF)[1]	10 dB
On-Chip Memory	16 MB
External Memory	Up to 2 GB LPDDR4 [Up to 32-bit @ 4266 MHz]
Compute Processing Cores	2 ARM Cortex-R5F CPUs @ 667 MHz
Digital Signal Processing (DSP) Cores	2 Tensilica-P5 DSPs @ 533 MHz
Chip Control Processor and Functional Safety Manager	ARM Cortex M0+ CPU @400 MHz with Lockstep Configuration
Security (Secure Boot, Interference, Updates)	Hardware Security Module (HSM)
I/O Interfaces	3 x 100/1000 Ethernet, 2 x CAN-FD, 2 x I2C, QSPI, GPIO
Power Consumption	Typical 9 W @ 50% Duty Cycle
Package	12.8 mm x 8.21 mm eWLB (wafer level chip scale package)
Temperature Range (Tj)	-40°C to +125°C

[1] Typical

Typical Application Block Diagram