

9.2 A 192-Virtual-Receiver 77/79GHz GMSK Code-Domain MIMO Radar System-on-Chip

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MIMO radars transmit selected waveforms on N TX physical antennas: when they receive them back on M RX physical antennas, they are able to reconstruct an array with $(N \times M)$ virtual receive elements, thereby obtaining a finer spatial/angular resolution. Fully integrated mm-wave radar transceivers such as [1-3] implement up to 12 Virtual Receivers (VRX) and can be expanded to larger time-domain MIMO arrays only by relying on costly PCB-based implementations.

We propose a code-domain MIMO radar capable of processing up to 192 VRX: we put special emphasis on architecting a platform that is sufficiently versatile to cover diverse applications, while still minimizing costs and meeting the most challenging link-budget requirements. Figure 9.2.1 shows the block diagram of the proposed radar: the SoC features a 77/79GHz-band transceiver with 12 TX and 8 RX channels that can be time-multiplexed to 2 sets of antennas to get coverage of both azimuth and elevation profiles. In this prototype, the 15.2-to-16.2GHz LO is generated by an external PLL: the differential LO input is converted to quadrature by using a polyphase filter (PPF); the filter output is buffered and distributed to all TX/RX channels with a differential 100Ω -terminated transmission line. Finally, all channels use limiting amplifiers and Sub-Harmonic Quadrature-Injection-Locked Oscillators (SH-QILO) to generate the mm-wave carrier at $5 \times$ the injected LO frequency. Digital signal processing and other radar signal computational power is supported on the same chip by two CPUs with floating point support and two DSPs. The overall software-defined hardware pipeline is capable of up to 20 Tera-Ops baseband processing.

Figure 9.2.2 shows the architecture of the proposed TX: a GMSK digital modulator feeds a zero-IF quadrature mm-wave upconverter. When compared to BPSK radar implementations [1], this TX is more spectrally efficient due to the absence of the large adjacent frequency sidelobes. Compared to FMCW radars [2], we shift the modulation complexity/precision to the high-speed data-converters and the DSP, where performance scales well with the CMOS technology node. A quadrature GMSK up-converter generates a constant-envelope phase-modulated signal and uses a fully saturated power amplifier. Code-domain MIMO allows to achieve more power on target by simultaneously using multiple TX channels with different codes. Hence, for a given link budget, designing smaller PAs becomes a viable option, which allows to more easily fulfill the most stringent lifetime requirements. Digital beamforming is an available mode of operation that allows to trade field of view for higher EIRP. At baseband, a programmable Pseudo-Random-Noise (PRN) code is generated, digitally GMSK modulated and fed into current-steering $2/4/8$ Gs/s DACs whose current outputs are amplified and filtered by reconstruction filters. The inset in Fig. 9.2.2 shows the schematic of this current-mode biquadratic filter: transistors M1p/m, M2p/m and M3p/m form a negative feedback that translates into a low input impedance at nodes iip and iim. Transistors M4p/m provide the scaled output current to the mixer. This architecture implements a current-mode gm-C biquad with programmable cut-off frequency (0.25 to 2GHz) and current gain (0 to 14dB). The current-mode double-balanced mixer performs the frequency upconversion to the 77/79 GHz bands.

The RX uses a zero-IF architecture followed by 2Gs/s SAR ADCs, a digital front-end and a data control unit, which handles the radar data cube computations including range correlation, doppler processing and beamforming. As shown in Fig. 9.2.3, the RX front-end is built around the 3-winding planar transformer T0. The first LNA stage is duplicated into LNA11 and LNA12: at their inputs, these amplifiers are connected to two different antenna ports while their outputs are power-combined into T0. This solution allows to time-multiplex the RX to azimuth or elevation antennas, avoiding the use of lossy mm-wave SPDT switches. The RX front-end needs to tackle a large modulated self-interference coming from the radar's own TXs, which may both saturate the RX and increase the correlation

noise floor. This challenge is even more stringent in MIMO radars where multiple TX active channels may constructively sum up at specific RX inputs. We propose a cancellation scheme comprising a Pattern Generator Unit (PGU), Analog and Digital Interference Cancellation Units (A/D-ICU). In the A-ICU, a background channel estimation runs continuously: the resulting signal path delays and impulse response are then applied to the upconverted mm-wave feedback whose output is power-combined into the transformer T0. The D-ICU estimates the complex sum of the wideband self-interferer presented at each receiver input and further removes the residual interferer before the correlators. The Radar Data Control Unit can process up to 1024 range bins for a single radar scan. The Winograd FFT engine can manage up to 800 million points per second Doppler throughput. The beam-forming engine throughput is 1.6 billion-beams/s and implements a covariance-matrix SVD decomposition engine that can support Direction-of-Arrival algorithms such as Multiple Signal Classification (MUSIC), Estimation of Signal Parameters via Rotational Invariance Techniques (ESPRIT) and Capon's algorithm engine to further improve the angular resolution.

The radar SoC prototype was implemented in a CMOS 28nm HPC technology and packaged in a Fan-Out Wafer-Level Package. The die micrograph is shown in Fig. 9.2.7: the SoC occupies 71mm^2 within which the mm-wave transceiver itself occupies 14mm^2 , resulting in one of the smallest-area per VRX to date. The overall power consumption varies with the use case and it is typically 15W from 0.9/1.3/1.8V supplies. The mm-wave RF characterization was performed on a test PCB with WR12 waveguide interfaces for each TX and RX channel. The radar is tested with an external PLL, and the 77.5GHz TX phase-noise at 1MHz offset is -110dBc/Hz .

Figure 9.2.4 shows measurement results for the RX self-interference cancellation unit. These system measurements were performed on an antenna board that uses Substrate-Integrated-Waveguide (SIW) antennas. During this test, 8 TXs were operating at the same time in MIMO mode. The resulting RX output is shown in the FFT, IQ and correlation domains, before and after cancellation. We report more than 30dB cancellation which allows to concurrently lower the correlation noise floor by about 20dB compared to when the self-interference is present.

Figure 9.2.5 shows 4 different static radar SoC measurements. Figure 9.2.5(a) shows a MIMO measurement for a car moving at 25 mph boresight on an air field: the radar graph shows 22dB SNR for an instantaneous detection at 290m. In Fig. 9.2.5(b) the radar is operating in phased-array mode and shows detections for a person moving boresight up to 280m. Figure 9.2.5(c) shows results of beamforming (dashed green line) and MUSIC (blue line) in an anechoic chamber: the radar resolves the two -10dBsm corner reflectors within about ± 1 -degree angle. Figure 9.2.5(d) shows how the digital beamforming sidelobe performance (red) can be improved after windowing (blue) and using a hardware-based Spatially-Variant Apodization (SVA) (green). The key mm-wave performance is provided in Fig. 9.2.6 together with a comparison with the recent state-of-the-art for PMCW/FMCW radars. At the package output reference plane, the TX combined output power is about $+19.6\text{dBm}$ (125C/80GHz), when 12 TX are active at the same time. The RX NF measured at the ADC output is about 16dB (125C/80GHz).

A MIMO radar SoC is presented that uses a novel digital-modulation architecture and achieves state-of-the-art mm-wave performance. The SoC achieves the best angular resolution, while being the most integrated CMOS radar sensing platform compared to the state of the art shown in Fig. 9.2.6.

Acknowledgements:

The authors would like to thank for their contributions A. Sengottuvel, Y. Ramasamy, M. Ali, A.E. Ertan, A. Sathyanarayana, R. Rao, J.P. Bordes, J. Preussner, and J. Schroeder.

References:

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- [2] B. P. Ginsburg et al., "A Multimode 76-to-81GHz Automotive Radar Transceiver with Autonomous Monitoring," *ISSCC*, pp. 158-160, 2018.
- [3] T. Fujibayashi et al., "A 76-to-81-GHz Multi-Channel Radar Transceiver," *IEEE JSSC*, vol. 52, no. 9, pp. 2226-2241, Sept. 2017.

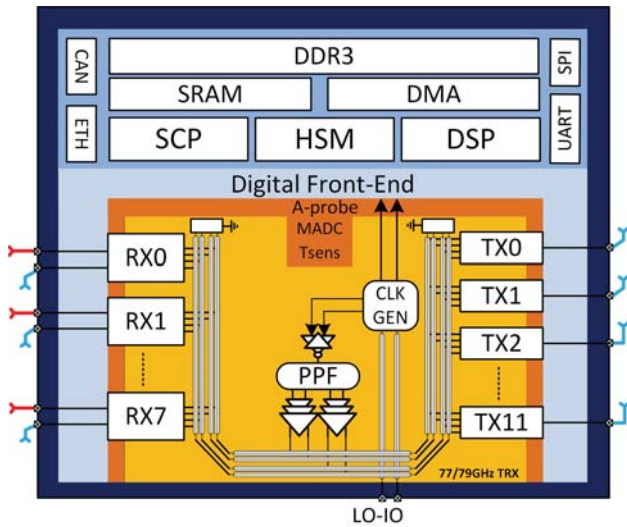


Figure 9.2.1: Radar SoC block diagram, including the 12TX / 8x2 RX 77/79 GHz MIMO transceiver, the digital signal processing, memory and interfaces.

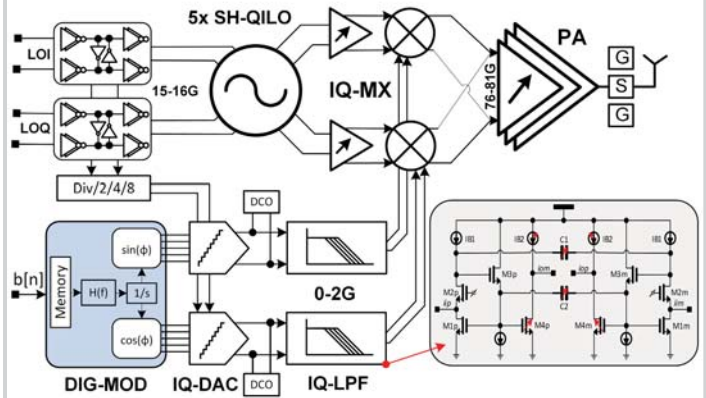


Figure 9.2.2: TX Block Diagram and schematic of the wideband current-mode biquadratic cell.

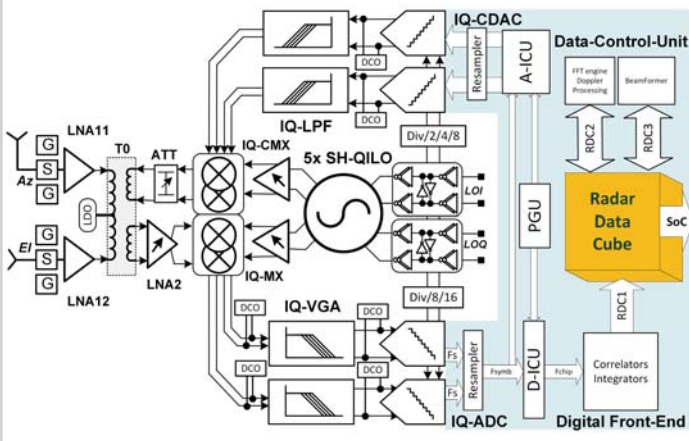


Figure 9.2.3: RX architecture, including details of the double-antenna-input LNA, the cancellation feedback, as well as the digital front-end.

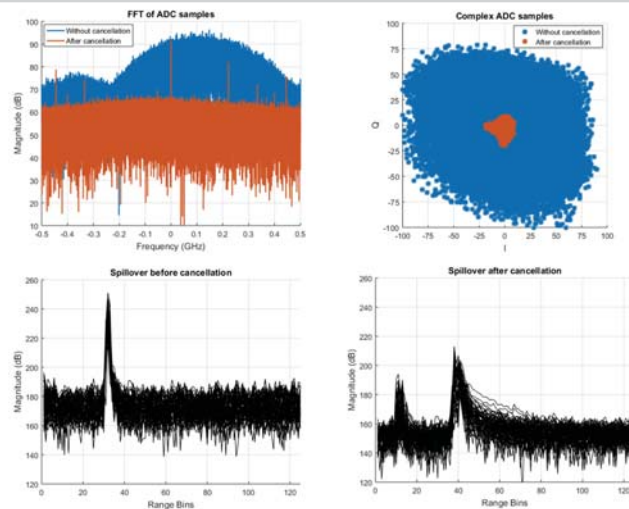


Figure 9.2.4: GMSK Spillover cancellation for 8 TX MIMO channels operating at the same time. The RX outputs are shown in the FFT, IQ and correlation domains before and after cancellation.

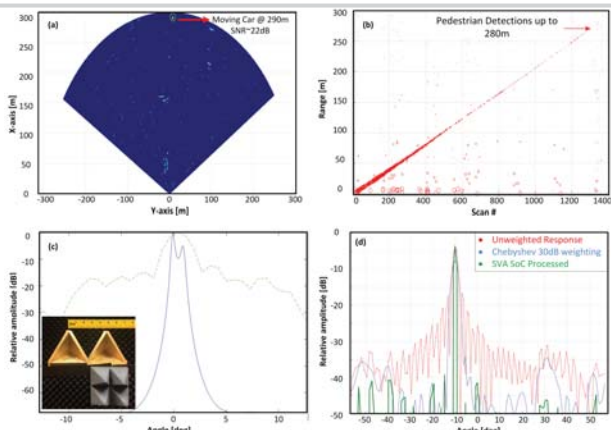


Figure 9.2.5: Radar-on-Chip measurements: (a) 25mph moving car MIMO detection at 290m with 22dB SNR; (b) Beamforming pedestrian detections up to 280m; (c) -10dBsm corner reflectors in anechoic chamber after beamforming and Music; (d) angle sidelobes performance after digital beamforming (red), using a Chebyshev window (blue) or applying Spatially-Variant Apodization (SVA) in hardware.

		This work	[1]	[2]	[3]
Technology		CMOS 28nm	CMOS 28nm	CMOS 45nm	SiGe 130nm
Modulation		GMSK-PMCW	BPSK-PMCW	FSK-FMCW	-
mm-wave bands		77/79 GHz	77/79 GHz	77/79 GHz	77/79 GHz
Physical mm-wave antenna IOs	#	12 / 8(x2) / 192	2 / 2 / 4	3 / 4 / 12	1 / 6 / 6
TX Max Combined Output Power	dBm	19.6	11.5	15.8	13
RX Noise Figure	dB	16	12	17.8	13.5
RX IP1dB	dBm	-6.7	-	-5	+3
RX IF BW	GHz	0.25 to 2	0.25 to 1	15	-
RF TRX summary					
TRX Silicon Area breakdown	mm ²	14	7.9	22	12
TRX Area / (# VRx)	mm ² /VRx	0.14 (96)	1.97 (4)	1.83 (12)	1 (12)
TRX Power consumption (3TX x 4RX, 12 VRx, 100%)	W	3.5	-	3.5	1.8
TRX Power consumption (12TX x 8RX, 96 VRx, 100%)	W	9.5	-	-	-
Power consumption / (# VRx)	mW/VRx	100 (96)	250 (4)	292 (12)	300 (6)
SoC system summary					
Range Resolution	cm	7.5	7.5	-	-
Angular Resolution	deg	1	5	-	-
Doppler Resolution	Km/h	0.099	-	-	-
Baseband processing	Tera-op/s	20	-	-	-
Total Silicon Area	mm ²	71	-	-	-
Typical Power Consumption	W	15	-	-	-

Figure 9.2.6: Summary and comparison for 125C/80GHz performance at the package output.

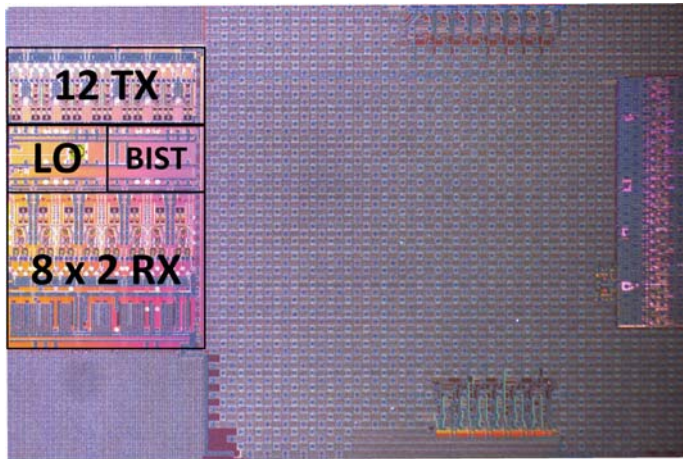


Figure 9.2.7: Die micrograph.